Review on Neutral Point Potential Balance Strategies for Three-Level Inverters

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Abstract: Three-level inverters possess the characteristics of higher voltage withstand, lower loss, lower harmonic and electromagnetic interference than two-level inverters. However, the neutral point potential fluctuation phenomenon not only causes the IGBT to withstand excessive voltage but also causes distortion of the output waveforms of the three-level inverters. This paper mainly discusses the imbalance of the neutral point potential under different modulation strategies of the three-level inverters and how to adjust can reduce the fluctuation of the neutral point potential.

1. Introduction

The neutral point potential imbalance increases the risk of breakdown of the switch and also increases the harmonic content of the inverters output waveforms [1-4]. Existing solutions to this problem can be divided into self-balancing methods, hardware solutions, and pulse width modulation based methods.

The self-balancing methods study the mechanism of self-balancing effect [5, 6], and point out that the effect depends on the switching frequency and current harmonics, then propose a method to enhance the self-balancing ability. Literature [7] designed a passive balancing circuit to enhance the self-balancing effect, as shown in Figure 1. The self-balancing neutral point potential control methods can only reduce the DC offset of the neutral point potential and require a large DC side capacitor to suppress the AC ripple of the neutral point potential.

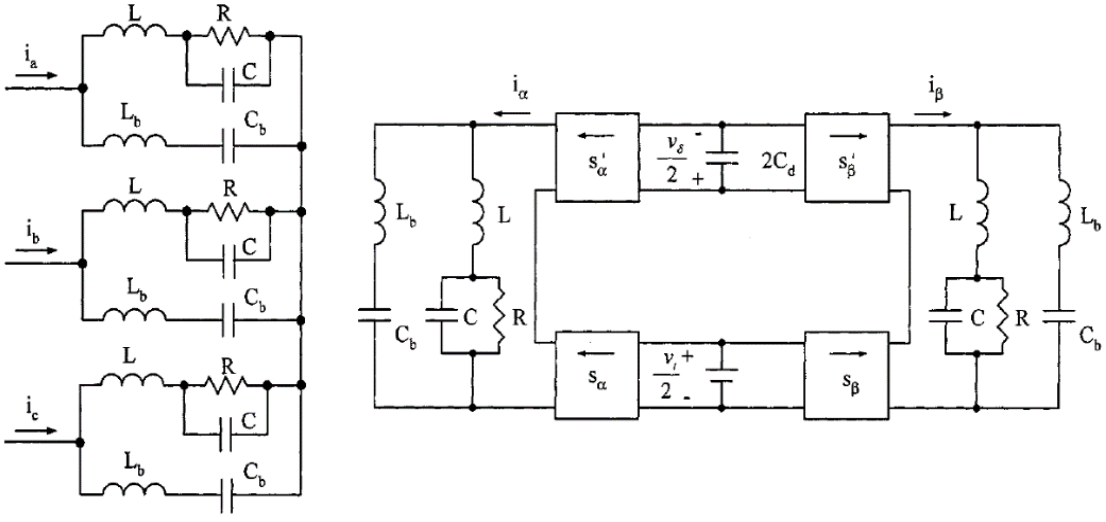

Figure 1. Three-level inverter equivalent circuit with balancing circuit

The hardware solutions completely eliminate the DC offset and AC ripple of the neutral point potential by means of an auxiliary hardware circuit or with two inverters. Literature [8] designed a balanced circuit based on the principle of DC-DC conversion, as shown in Figure 2. The hardware-based neutral point potential balancing methods do not require changes to the PWM strategies and are the most effective of all neutral point potential control methods. Nevertheless, these methods will increase the cost and the size of the inverters.

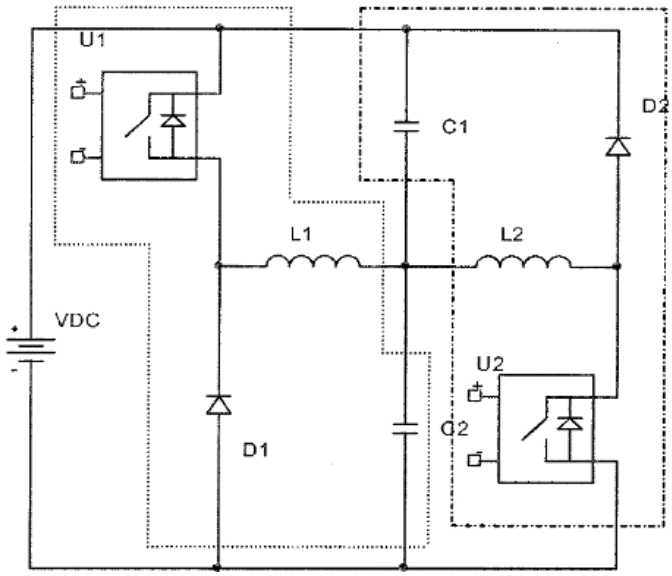

Figure 2. Balance circuit based on DC-DC conversion principle

The pulse width modulation based methods eliminate the DC offset and AC ripple of the neutral point potential by adjusting the switching strategy. These methods can be divided into space vector pulse width modulation and sinusoidal pulse width modulation. Space vector pulse width modulation is widely used due to higher bus voltage utilization, which can also be divided into the nearest three vector pulse width modulation (NTVPWM) [9] and virtual space vector pulse width modulation (VSVPWM) [10].

The self-balancing methods belong to the passive-control and the methods based on the hardware schemes are costly. At present, the three-level neutral point potential control mainly adopt methods based on pulse width modulation. These methods are active-control and do not require additional hardware circuitry. This paper mainly discusses the principle of the neutral point potential fluctuation caused by the NTVPWM and VSVPWM.

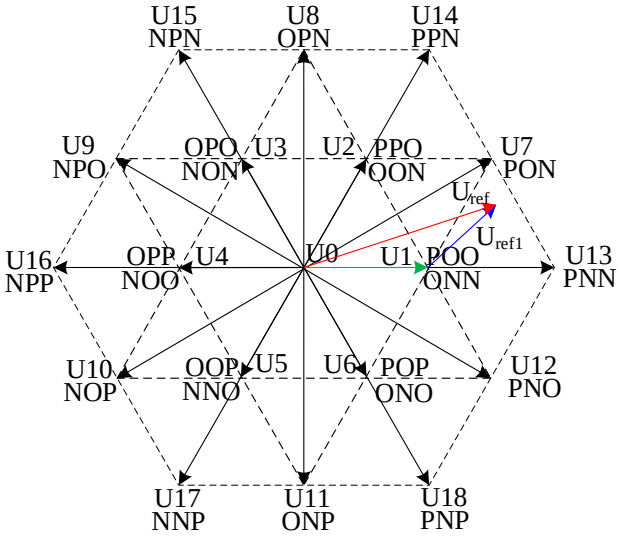

Figure 3. Voltage vector diagram of three-level inverters

2. The NTVPWM

Existing researches generally believe that the neutral point potential imbalance will increase the voltage stress of the switching device and cause the output waveform of the inverters. The former effect is obvious and unquestionable, but the latter effect is very different for NTVPWM and VSVPWM, as analyzed below.

The neutral point potential control strategy based on NTVPWM balances the neutral point

potential by adjusting the action time of the redundant small vectors. Figure 3 shows voltage vector diagram of three-level inverters and figure 4 is a vector diagram of the voltage of NTVPWM in sector 1.

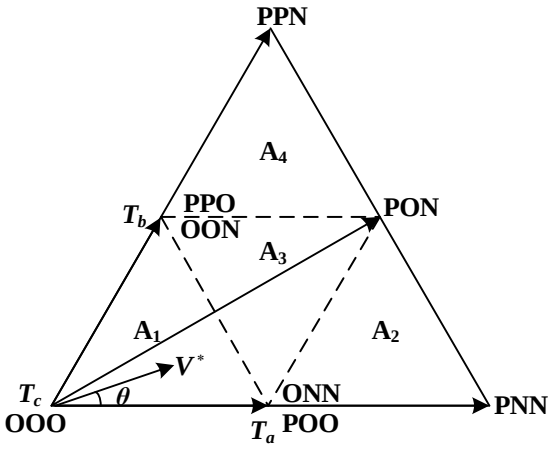

Figure 4. Voltage vector in sector 1 of NTVPWM

The action time of each voltage vector in sector 1 sub-sector A_1 is as follows:

$$\begin{aligned} t_{ONN} &= k_1 T_a \\ t_{POO} &= (1-k_1) T_a \\ t_{OON} &= k_2 T_b \\ t_{PPO} &= (1-k_2) T_b \\ t_{OOO} &= T_c \end{aligned} \tag{1}$$

Where k_1 and k_2 are the partition coefficients of the two pairs of redundant small vectors ONN/POO and OON/PPO action times, respectively.

For the original NTVPWM, $k_1 = 0.5$, $k_2 = 1$ ($\theta \in (0^\circ, 30^\circ)$). NTVPWM under hysteresis control, k_1 and k_2 switch between 0 and 1. NTVPWM under PID control, k_1 and k_2 are adjusted between 0 and 1. If a PWM strategy is not affected by the neutral point potential imbalance, then the following formula holds:

$$t_{ao} = t_{bo} = t_{co} \tag{2}$$

Obviously, for the above three switching strategies, the formula (2) cannot always be established. So when the motor is started, the imbalance of the neutral point potential will cause the torque to pulsate.

3. The VSVPWM

For VSVPWM, k_1=0.5, k_2=0.5, so in the sub-sector A_1, the equation (2) always holds. In the other sub-sectors of sector 1, equation (2) also holds and the proof process is as follows. The expression of the duty cycle based on VSVPWM in 0-60 degrees is as:

$$\begin{aligned} d_{ap} &= m\cos(\theta - \pi/6) \\ d_{an} &= 0 \\ d_{bp} &= m\cos(\theta - \pi/2) \\ d_{bn} &= m\cos(\theta + \pi/6) \\ d_{cp} &= 0 \\ d_{cn} &= m\cos(\theta - \pi/6) \end{aligned} \tag{3}$$

The duty ratio of the three levels of each phase satisfies the following constraint relationship:

$$d_{ip} + d_{io} + d_{in} = 1, \quad i = a, b, c \tag{4}$$

From the expression (3) and (4), the equation can be derived as follows:

$$d_{ao} = d_{bo} = d_{co} \tag{5}$$

As can be seen from the above equation, VSVPWM will not cause voltage distortion due to neutral point potential imbalance or even DC side capacitor damage. Compared to NTVPWM, VSVPWM is much more robust to neutral point potential imbalance.

4. Conclusion

This paper mainly discusses the phenomenon of neutral point potential fluctuation in three-level inverters based on pulse width modulation strategy. The principle and the same and different points of the NTVPWM and VSVPWM are given. In general, the NTVPWM algorithm has the switching states that can cause the neutral point potential to fluctuate. The VSVPWM algorithm theoretically does not have the possibility of causing the neutral point potential fluctuation, but will increase the switching frequency of the IGBT and bring the extra losses.

Acknowledgments

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